REMARKS

Claims 1, 5, 10-13, 16 and 19 have been amended to improve form and claims 8, 14 and 20 have been canceled without prejudice or disclaimer. Claims 1-7, 9-13 and 15-19 are now pending in this application.

Claims 1, 2, 4-6, 9-11 and 13-18 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Runaldue et al. (U.S. Patent No. 6,052,751; hereinafter Runaldue) in view of Scheuneman et al. (U.S. Patent No. 4,652,993; hereinafter Scheuneman) and claims 3, 7, 8, 12, 19 and 20 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Runaldue in view of Scheuneman and further in view of Springer et al. (U.S. Patent No. 4,247,920; hereinafter Springer). The rejections are respectfully traversed.

Claim 1 recites a network switch that includes a plurality of receive devices and an external memory interface. Claim 1 recites that the external memory interface is configured to receive data from the plurality of receive devices, transfer a portion of the data received from a first one of the receive devices to a first memory, and transfer a portion of the data received from a second one of the receive devices to a second memory. The Office Action admits that Runaldue does not disclose these features, but states that Scheuneman discloses these features and points to Fig. 1a, elements 1a to 3a and 1b to 3b and col. 17, lines 60-64 for support (Office Action – pages 2-3). The applicants respectfully disagree.

Scheuneman discloses a high performance memory unit for simultaneously reading data from a number of independently operative memory banks (Scheuneman – Abstract). Scheuneman at Fig. 1a, illustrates a number of memory banks 3a to 3h connected to output ports a-d (elements 1a-1d) via multiplexers 2a-2d. Scheuneman at col. 17, lines 60-64 discloses that the invention is directed to a method and apparatus for the simultaneous

movement of data read from a number of memory banks to a number of output data ports. These portions of Scheuneman, or any other portions of Scheuneman, do not disclose or suggest an external memory interface configured to receive data from a plurality of receive devices, transfer a portion of the data received from a first one of the receive devices to a first memory and transfer a portion of the data received from a second one of the receive devices to a second memory, as recited in claim 1. Rather, these portions of Scheuneman disclose reading data from a number of memory banks for transfer to a number of output ports.

Claim 1, as amended, also recites that the external memory interface includes a first external memory bus to transfer data to the first memory and a second external memory bus to transfer data to the second memory. These features were previously recited in claim 8. As to these features, the Office Action states that Scheuneman discloses these features and points to col. 45, lines 5-11 of Scheuneman for support (Office Action – page 8). The applicants respectfully disagree.

As discussed above, Scheuneman discloses transferring data from a number of memory banks to a number of output ports. Scheuneman at col. 45, lines 5-11 discloses that multiple wired-OR communication buses may be connected from the memory banks to the output ports. This is not equivalent to a first external memory bus to transfer data to the first memory and a second external memory bus to transfer data to the second memory, as recited in claim 1. Once again, this portion of Scheuneman is directed to transferring data from the memory banks, not to the memory banks, as required by claim 1.

Claim 1, as amended, further recites that the external memory interface is further configured to generate odd address information when transferring data via the first external

memory bus and even address information when transferring data via the second external memory bus. This feature was also previously recited in claim 8.

As to this feature, the Office Action admits that Scheuneman does not disclose this feature, but states that Springer discloses using two memories, one being used for even memory storage and the other being used for odd memory storage and points to col. 4, lines 14-31 of Springer for support (Office Action – page 9).

Springer is directed to a system for permitting individual bytes of a two-byte information signal to be stored or retrieved from a single memory space (Springer – col. 1, lines 40-58). Springer at col. 4, lines 14-43 discloses that in response to an 8-bit mode signal, control circuit 38 disables incrementor 36 to permit the upper 15 bits of the address signal to be passed to even memory module 24 and that the 15-bit address is applied directly to odd memory module 22 directly from line 34. This portion of Springer also discloses that if the least significant bit of the address signal is a "0," the access is to the even memory module 24 and only that memory module is activated to receive a data signal from mux 28 for a write operation. If the least significant bit of the address is a "1," only the odd memory module 22 is activated. In summary, this portion of Springer merely discloses that the least significant bit of an address signal determines which memory module is activated. This is not equivalent to and does not suggest an external memory interface that is configured to generate odd address information when transferring data via the first external memory bus and even address information when transferring data via the second external memory bus, as recited in amended claim 1. In other words, Springer does not disclose or suggest generating odd or even address information, but merely uses the existing address information to determine which memory module is activated.

For at least the reasons discussed above, the combination of Runaldue, Scheuneman and Springer does not disclose or suggest each of the features of claim 1. Accordingly, withdrawal of the rejection and allowance of claim 1 are respectfully requested.

Claims 2-7 and 9 are dependent on claim 1 and are believed to be allowable for at least the reasons claim 1 is allowable. In addition, these claims recite additional features not disclosed or suggested by the cited art.

For example, claim 2 recites that the external memory interface includes a scheduler coupled to the receive devices and configured to enable the received data frames to be output to the first and second memories, the scheduler simultaneously outputting first and second selection signals for outputting data from the first receive device and the second receive device, respectively. The Office Action states that Scheuneman discloses "that the switch transfers a portion of the data received from a first one of the receive devices to a first memory, while you can transfer a portion of the data received from a second one of the receive devices to a second memory" and points to Fig. 1a and col. 17, lines 60-64 for support (Office Action – page 3). These portions of Scheuneman, as discussed above, disclose reading data from a number of memory banks for transfer to a number of output ports. These portions of Scheuneman do not disclose or suggest simultaneously outputting first and second selection signals for outputting data from the first receive device and the second receive device, as required by claim 2. Therefore, even if Scheuneman was combined with Runaldue, the combination would still not disclose or suggest a scheduler that simultaneously outputs first and second selection signals for outputting data from the first receive device and the second receive device, respectively.

For at least these additional reasons, withdrawal of the rejection and allowance of claim 2 are respectfully requested.

Claim 5 recites that the external memory interface is configured to simultaneously transfer data received from a first one of a first group of the receive devices via the first external memory bus and a second one of a second group of the receive devices via the second external memory bus. The Office Action states that Scheuneman discloses this feature and points to col. 45, lines 5-11 for support (Office Action – page 4). The applicants respectfully disagree.

Scheuneman at col. 45, lines 5-11 discloses that a wired-OR communication bus may be connected from the even memory banks to the output ports and that a second wired-OR communication bus may be connected from the odd memory banks to the output ports. This is not equivalent to simultaneously transferring data received from a first one of a first group of the receive devices via the first external memory bus and a second one of a second group of the receive devices via the second external memory bus. In contrast, this portion of Scheuneman does not even disclose transferring data from a receive device to a memory device, much less simultaneously transferring data from a first one of a first group of receive devices via a first external memory bus and a second one of a second group of received devices via the second external memory bus, as required by claim 5.

For at least these additional reasons, withdrawal of the rejection and allowance of claim 5 are respectfully requested.

Claim 10, as amended, recites temporarily storing the received data frames in a plurality of receive devices. Claim 10, as amended, further recites simultaneously transferring data frame information to at least a first memory and a second memory, wherein

the simultaneously transferring includes alternately transferring data frame information from a first group of the receive devices to the first and second memories and alternately transferring data frame information from a second group of the receive devices to the first and second memories. This feature was previously recited in claim 14.

The Office Action states that Scheuneman discloses these features and points to Fig. 1a of Scheuneman for support. In particular, the Office Action states that "the first device, 1a, goes through the multiplexer 2a and can send to any memory unit and the second device, 1b, goes through the multiplexer 2b and can travel to any storage unit, so the interface is configured to transfer data to the first or second memory unit for each device" (Office Action – page 6).

First, Scheuneman, as discussed above, discloses reading data from memory banks 3a-3h via multiplexers 2a-2d for transfer to output ports 1a-1d. Scheuneman does not disclose or suggest transferring data to a first and second memory, as required by claim 10.

Secondly, even if, for the sake or argument, Scheuneman was construed to disclose transferring data to a first and second memory, Scheuneman does not disclose that the simultaneously transferring includes alternately transferring data frame information from a first group of the receive devices to the first and second memories and alternately transferring data frame information from a second group of the receive devices to the first and second memories, as recited in amended claim 10. For example, even if the output ports of Scheuneman were construed to be equivalent to a group of receive devices, Scheuneman does not disclose or suggest grouping the output ports in first and second groups, as required by claim 10. Scheuneman, therefore, cannot disclose alternately

transferring data frame information from the first and second groups to the first and second memories, as further required by claim 10.

For at least these reasons, the combination of Runaldue and Scheuneman does not disclose or suggest each of the features of claim 10. Accordingly, withdrawal of the rejection and allowance of claim 10 are respectfully requested.

Claims 11-13 and 15 are dependent on claim 10 and are believed to be allowable for at least the reasons claim 10 is allowable. Accordingly, withdrawal of the rejection and allowance of claims 11-13 and 15 are respectfully requested.

Claim 16 recites a data communication system that includes a plurality of receive devices, a scheduler and a switching device. The switching device is configured to receive the data frame information and to simultaneously transfer data frame information from a first one of the data frames via a first external memory bus and data frame information from a second one of the data frames via a second external memory bus.

Claim 16, as amended, also recites a first memory configured to receive data frame information from the first external memory bus and a second memory configured to receive data frame information from the second external memory bus. This feature was previously recited in claim 19. With respect to a similar feature recited in original claim 1, the Office Action states that Scheuneman discloses transferring data received from a first receive device to a first memory and transferring data from a second receive device to a second memory and points to Fig. 1a and col. 17, lines 60-64 for support (Office Action – pages 2-3).

As discussed above with respect to claim 1, these portions of Scheuneman disclose reading data from a number of memory banks for transfer to a number of output ports. These portions of Scheuneman do not disclose or suggest a first memory configured to receive data frame information from a first external memory bus and a second memory configured to receive data frame information from a second external memory bus, as recited in amended claim 16.

Claim 16, as amended, further recites that the switching device is further configured to generate data address information having odd addresses for data transferred to the first memory and generate data address information having even addresses for data transferred to the second memory. This feature was previously recited in claim 20. As to this feature, the Office Action states that Springer discloses using odd and even memories and generating odd addresses for data transferred to a first memory and even addresses for data transferred to a second memory and points to col. 4, lines 14-31 of Springer for support (Office Action – page 10). The applicants respectfully disagree.

These portions of Springer, as discussed above with respect to claim 1, merely disclose that the least significant bit of an address signal determines which memory module is activated. This is not equivalent to and does not suggest generating data address information having odd addresses for data transferred to the first memory and generating data address information having even addresses for data transferred to the second memory, as recited in claim 16. In other words, Springer does not disclose or suggest generating odd or even address information, but merely uses the existing address information to determine which memory module is activated.

For at least these reasons, the combination of Runaldue, Scheuneman and Springer does not disclose or suggest each of the features of claim 16. Accordingly, withdrawal of the rejection and allowance of claim 16 are respectfully requested.

Claims 17-19 are dependent on claim 16 and are believed to be allowable for at least the reasons claim 16 is allowable. In addition, these claims recite additional features not disclosed or suggested by the cited art.

For example, claim 18 recites that the switching device is further configured to alternately transfer data received from the first multiplexer to the first and second external memory buses and to alternately transfer data received from the second multiplexer to the first and second external memory buses. The Office Action states that Scheuneman discloses this feature and points to Fig. 1a for support (Office Action – pages 7-8). The applicants respectfully disagree.

This portion of Scheuneman, as discussed above, merely discloses reading data from a number of memory banks for transfer to a number of output ports. This is not equivalent to and does not suggest alternately transferring data received from the first multiplexer to the first and second external memory buses and alternately transferring data received from the second multiplexer to the first and second external memory buses, as recited in claim 18.

For at least these additional reasons, withdrawal of the rejection and allowance of claim 18 are respectfully requested.

CONCLUSION

In view of the foregoing amendments and remarks, the applicants respectfully request withdrawal of the outstanding rejections and the timely allowance of this application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Date: January 5, 2004

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